REMARKS

Claims 1-5, 8-10, 12-15, 17, 19, and 21-22 are pending. The Office Action dated August 24, 2006, in this Application has been carefully considered. The above amendments and the following remarks are presented in a sincere attempt to place this Application in condition for allowance. Claims 1-5, 8-10, 12-15, 17, 19, and 21-22 have been amended, and claims 6-7, 11, 16, 18, 20, and 23-30 have been canceled in this Response. Reconsideration and allowance are respectfully requested in light of the above amendments and the following remarks.

Claims 1, 4, 12, 13, 29, and 30 were provisionally rejected under the judicial doctrine of non-statutory (obviousness-type) double patenting, the Examiner noting that claims 1, 2, 14, 21, 24, and 25 of U.S. Patent Application Serial No. 10/809,579 contain every element of those claims. In response thereto, Applicant notes that claims 29 and 30 are canceled herein. With regard to pending claims 1, 4, 12, and 13, Applicant is prepared to address the provisional double patenting rejection as and when the claims of U.S. Patent Application Serial No. 10/809,579 are allowed.

Claims 1-11, 16, and 22 were objected to due to informalities. In response thereto, Applicant notes that claims 6-7, 11, and 16 are canceled herein, and claims 1-5, 8-10, and 22 are amended herein. In pending claims 3-5 and 9-10, Applicant has replaced "where" with "wherein" as the Examiner suggested. Applicant believes amended claims 1-5, 8-10, and 22 are in condition for allowance.

Claims 29 and 30 were was rejected under 35 U.S.C. 101 as being directed to non-statutory subject matter. In response thereto, Applicant notes claims 29 and 30 are canceled herein.

Claim 7 was rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. In response thereto, Applicant notes claim 7 is canceled herein.

Claims 2, 3, 7, 17, and 24-26 were rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the applicant regards as the invention. In response thereto, Applicant notes that claims 7 and 24-26 are canceled herein. Applicant also notes claims 2, 3, and 17 are amended herein, and Applicant believes amended claims 2, 3, and 17 are in condition for allowance.

Claims 1-6, 8, 9-13, 15-18, and 20-28 were rejected under 35 U.S.C. 102(b) as being unpatentable over Patterson and Hennessey [Computer Architecture: A Quantitative Approach] (hereinafter "Patterson"). Applicant notes claims 6, 11, 16, 18, 20, and 23-28 are canceled herein, and respectfully traverses this rejection as it applies to claims 1-5, 8, 9-10, 12-13, 15, 17, and 21-22.

With regard to claims 1-5, 8, and 9-10, Patterson does not teach or disclose a processing system, including: a memory comprising a coherence directory and associated coherence directory data, wherein the coherence directory comprises a plurality of memory blocks each having different directory data; a plurality of buffers interconnected to the memory; a plurality of processing elements, each of the processing elements coupled to a different one of the plurality of buffers; wherein each of the processing elements comprises requesting means for requesting a selected one of the memory blocks from the memory; wherein the memory comprises ***means responsive to the requesting means, for providing the selected memory block and the coherence directory data corresponding to the selected memory block to a requesting one of the processing elements***; and wherein each of the processing elements comprises ***means for receiving the selected memory block and the coherence directory data corresponding to the selected memory block, and for determining if the selected memory block is available for a particular access mode***.

As amended herein, claim 1 recites (emphasis added):

1. A processing system, comprising:

a memory comprising a coherence directory and associated coherence directory data, wherein the coherence directory comprises a plurality of memory blocks each having different directory data;

a plurality of buffers interconnected to the memory;

a plurality of processing elements, each of the processing elements coupled to a different one of the plurality of buffers;

wherein each of the processing elements comprises requesting means for requesting a selected one of the memory blocks from the memory;

wherein the memory comprises means responsive to the requesting means, for providing the selected memory block and the coherence directory data corresponding to the selected memory block to a requesting one of the processing elements; and

wherein each of the processing elements comprises means for receiving the selected memory block and the coherence directory data corresponding to the selected memory block, and for determining if the selected memory block is available for a particular access mode.

Claim 1 recites "wherein the memory comprises means responsive to the requesting means, for providing the selected memory block and the coherence directory data corresponding to the selected memory block to a requesting one of the processing elements." In the Office Action, the Examiner points to "...the section Directory-Based Cache-Coherence Protocols: The Basics, pages 679-685." Patterson is a computer architecture textbook that generally describes directory-based cache-coherence protocols. Applicant asserts that Patterson does not teach or suggest a processing system "wherein the memory comprises means responsive to the requesting means, for providing ***the selected memory block and the coherence directory data corresponding to the selected memory block*** to a requesting one of the processing elements." Applicant also notes that none of the messages sent among nodes to maintain coherence described by Patterson include "***the selected memory block and the coherence directory data corresponding to the selected memory block***."

Claim 1 also recites "wherein each of the processing elements comprises means for receiving the selected memory block and the coherence directory data corresponding to the selected memory block, and for determining if the selected memory block is available for a particular access mode." In the Office Action, the Examiner points to "...the state transitions in Figs. 8.24 and 8.25

and explanations paragraphs in page 683, 684, and 685 illustrate updating the directory to enforce coherency as accesses of difference access modes are requested." Applicant asserts that Patterson does not teach or suggest a processing system "wherein each of the processing elements comprises means for means for receiving ***the selected memory block and the coherence directory data corresponding to the selected memory block***, and for determining if the selected memory block is available for a particular access mode." Applicant again notes that none of the messages sent among nodes to maintain coherence described by Patterson include "***the selected memory block and the coherence directory data corresponding to the selected memory block***."

For at least the above reasons, Applicant asserts Patterson fails to teach or disclose all of the elements and limitations of pending independent claim 1. Applicant also believes that pending claims 2-5 and 8-10 that depend from claim 1 are also allowable for at least the above reasons.

Applicant notes claims 13, 15, 17, and 21-22 depend from claim 12. With regard to claim 12, Applicant asserts Patterson does not teach or disclose a method for providing memory data to a requestor of the memory data, wherein the method includes requesting a memory block from a memory hierarchy level having a coherence directory and associated coherence directory data; ***generating a response including the memory data and corresponding coherence directory data***; updating the coherence directory data corresponding to the memory data; ***receiving the response including the memory data and the corresponding coherence directory data from the memory hierarchy level***; determining whether the received coherence directory data is compatible with a required access mode; performing at least one coherence action if the received coherence directory data is incompatible with the required access mode; and providing the memory data to the requestor of the memory data.

As amended herein, claim 12 recites (emphasis added):

12. A method for providing memory data to a requestor of the memory data, the method comprising:
    requesting a memory block from a memory hierarchy level having a coherence directory and associated coherence directory data;
    generating a response including the memory data and corresponding coherence directory data;

updating the coherence directory data corresponding to the memory data;

receiving the response including the memory data and the corresponding coherence directory data from the memory hierarchy level;

determining whether the received coherence directory data is compatible with a required access mode;

performing at least one coherence action if the received coherence directory data is incompatible with the required access mode; and

providing the memory data to the requestor of the memory data.

Claim 12 recites "generating a response including the memory data and corresponding coherence directory data." In the Office Action, the Examiner points to "...messages sent among nodes to maintain coherence, see page 681 and Fig. 8.23 [of Patterson]..." Applicant asserts that Patterson does not teach or suggest "generating a response including memory data and corresponding coherence directory data." None of the messages sent among nodes to maintain coherence described by Patterson on page 681 and in Fig. 8.23 include "memory data and corresponding coherence directory data" as recited in claim 12.

Claim 12 also recites "receiving a response including the memory data and the corresponding coherence directory data from the memory hierarchy level." In the Office Action, the Examiner again points to "...messages sent among nodes to maintain coherence, see page 681 and Fig. 8.23 [of Patterson]..." Applicant asserts that Patterson does not teach or suggest "receiving a response including the memory data and the corresponding coherence directory data from said memory hierarchy level." Again, none of the messages sent among nodes to maintain coherence described by Patterson on page 681 and in Fig. 8.23 include "memory data and the corresponding coherence directory data from said memory hierarchy level" as recited in claim 12.

For at least the above reasons, Applicant asserts Patterson fails to teach or disclose all of the elements and limitations of pending independent claim 12. Applicant also believes that pending claims 13-15, 17, 19, and 21-22 that depend from claim 12 are also allowable for at least the above reasons.

Claims 7, 14, 19, 29, and 30 were rejected under 35 U.S.C. 103(a) as being unpatentable over Patterson. Applicant notes claims 7 and 29-30 are canceled herein, and respectfully traverses this rejection as it applies to claims 14 and 19.

Claims 14 and 19 depend from claim 12 (reproduced above). With regard to claim 12, Applicant again asserts Patterson does not teach or disclose a method for providing memory data to a requestor of the memory data, wherein the method includes requesting a memory block from a memory hierarchy level having a coherence directory and associated coherence directory data; ***generating a response including the memory data and corresponding coherence directory data***; updating the coherence directory data corresponding to the memory data; ***receiving the response including the memory data and the corresponding coherence directory data from the memory hierarchy level***; determining whether the received coherence directory data is compatible with a required access mode; performing at least one coherence action if the received coherence directory data is incompatible with the required access mode; and providing the memory data to the requestor of the memory data.

As pointed out above, claim 12 recites "generating a response including the memory data and corresponding coherence directory data." Applicant again asserts that none of the messages sent among nodes to maintain coherence described by Patterson include "memory data and corresponding coherence directory data" as recited in claim 12.

Claim 12 also recites "receiving a response including the memory data and the corresponding coherence directory data from the memory hierarchy level." Applicant again asserts that none of the messages sent among nodes to maintain coherence described by Patterson include

"memory data and the corresponding coherence directory data from said memory hierarchy level" as recited in claim 12.

For at least the above reasons, Applicant asserts Patterson fails to teach or disclose all of the elements and limitations of pending independent claim 12. Applicant also believes that pending claims 13-15, 17, 19, and 21-22 that depend from claim 12 are also allowable for at least the above reasons.

In the present response, Applicant addresses all of the claim objections and rejections cited in the Office Action. In view of the amendments to the claims and Applicant's remarks, Applicant believes pending claims 1-5, 8-10, 12-15, 17, 19, and 21-22 are in condition for allowance, and respectfully request allowance of pending claims 1-5, 8-10, 12-15, 17, 19, and 21-22.

With the amendments to the claims presented herein, there are currently 2 pending independent claims and 16 total pending claims in the application. As the original application had 5 independent claims and 30 total claims, Applicant believes no additional fees are due. In the event that any other fees are due, the Commissioner is hereby authorized to charge any required fees due (other than issue fees), and to credit any overpayment made, in connection with the filing of this paper to Deposit Account No. 50-0605 of CARR LLP.

The present amendment is believed to contain a complete response to the issues raised in the Office Action. Full reconsideration is respectfully requested. If the Examiner should have any questions, comments or suggestions, the undersigned attorney earnestly requests a telephone conference. In particular, should the Examiner deem that any further amendment is desirable to place this application in condition for allowance, the Examiner is also invited to telephone the undersigned at the number listed below.

Respectfully submitted,

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